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Kim

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(54) **METHOD OF MANUFACTURING AN ORGANIC LIGHT EMITTING DISPLAY**

(71) Applicant: **Samsung Display Co., Ltd.**, Yongin, Gyeonggi-Do (KR)

(72) Inventor: **Eun-Ah Kim**, Yongin (KR)

(73) Assignee: **Samsung Display Co., Ltd.**, Giheung-Gu, Yongin, Gyeonggi-Do (KR)

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CPC **H01L 27/3253** (2013.01); **H01L 27/3244** (2013.01); **H01L 27/3251** (2013.01)

(58) **Field of Classification Search**

CPC H01L 31/1013; H01L 27/14601; H01L 27/14609; H01L 27/3244; H01L 27/12; H01L 2251/5315; H01L 27/3246; H01L 27/1255; H01L 27/15; H01L 27/3258; H01L

27/1248; H01L 27/13; H01L 27/3276; H01L 28/40; H01L 29/49; H01L 27/1214; H01L 27/3265; H01L 27/3248; H01L 27/326; H01L 27/3262; H01L 51/5253; H01L 29/4908; H01L 29/51; H01L 51/107; H01L 51/52

USPC 313/498-512; 427/66, 532-535, 539; 257/40, 72, 98-100, 642-643, 759; 445/25, 26

See application file for complete search history.

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Primary Examiner — Bao Q Truong

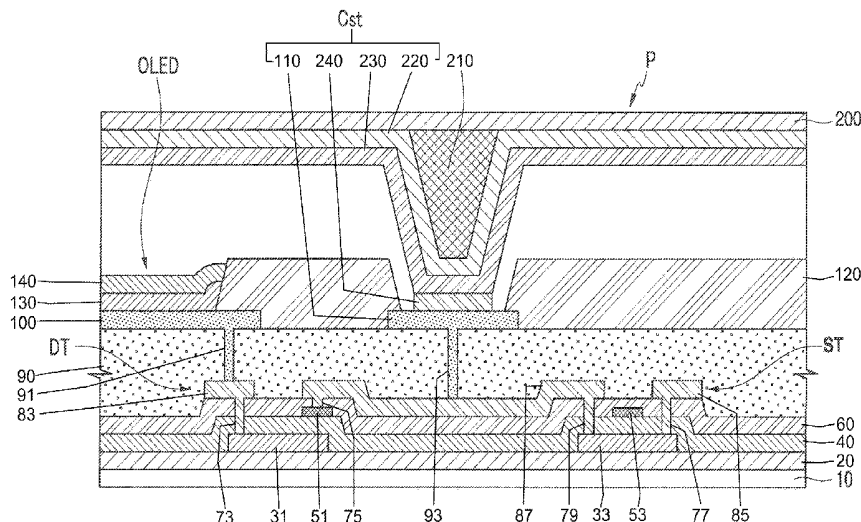
Assistant Examiner — Fatima Farokhrooz

(74) *Attorney, Agent, or Firm* — Robert E. Bushnell, Esq.

(57) **ABSTRACT**

An organic light emitting display resulting in an improved aperture ratio and a manufacturing method thereof. The organic light emitting display that includes a plurality of pixels arranged between first and second substrates, each of said pixels includes a plurality of thin film transistors, an organic light emitting diode, and a capacitor. The thin film transistors and the organic light emitting diode are formed on the first substrate and the capacitor is formed on the second substrate, and the thin film transistors and the capacitor are electrically connected with each other upon the first substrate being bonded to the second substrate.

20 Claims, 15 Drawing Sheets



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FIG. 1

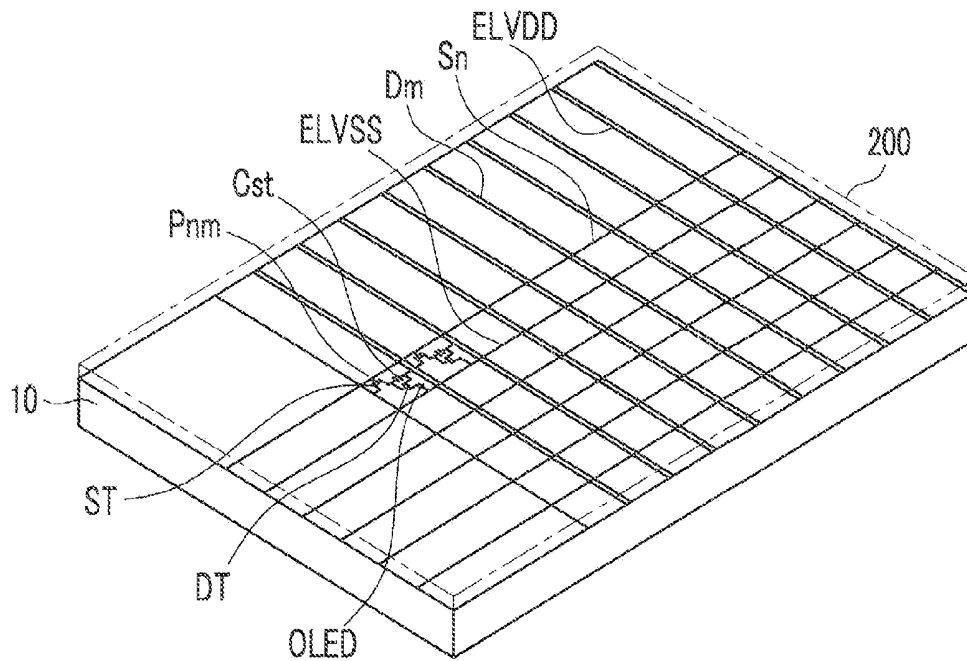
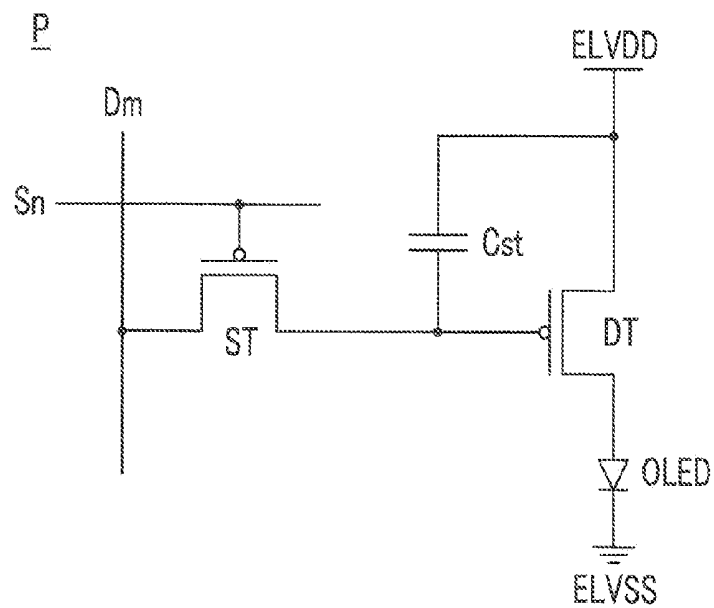


FIG. 2



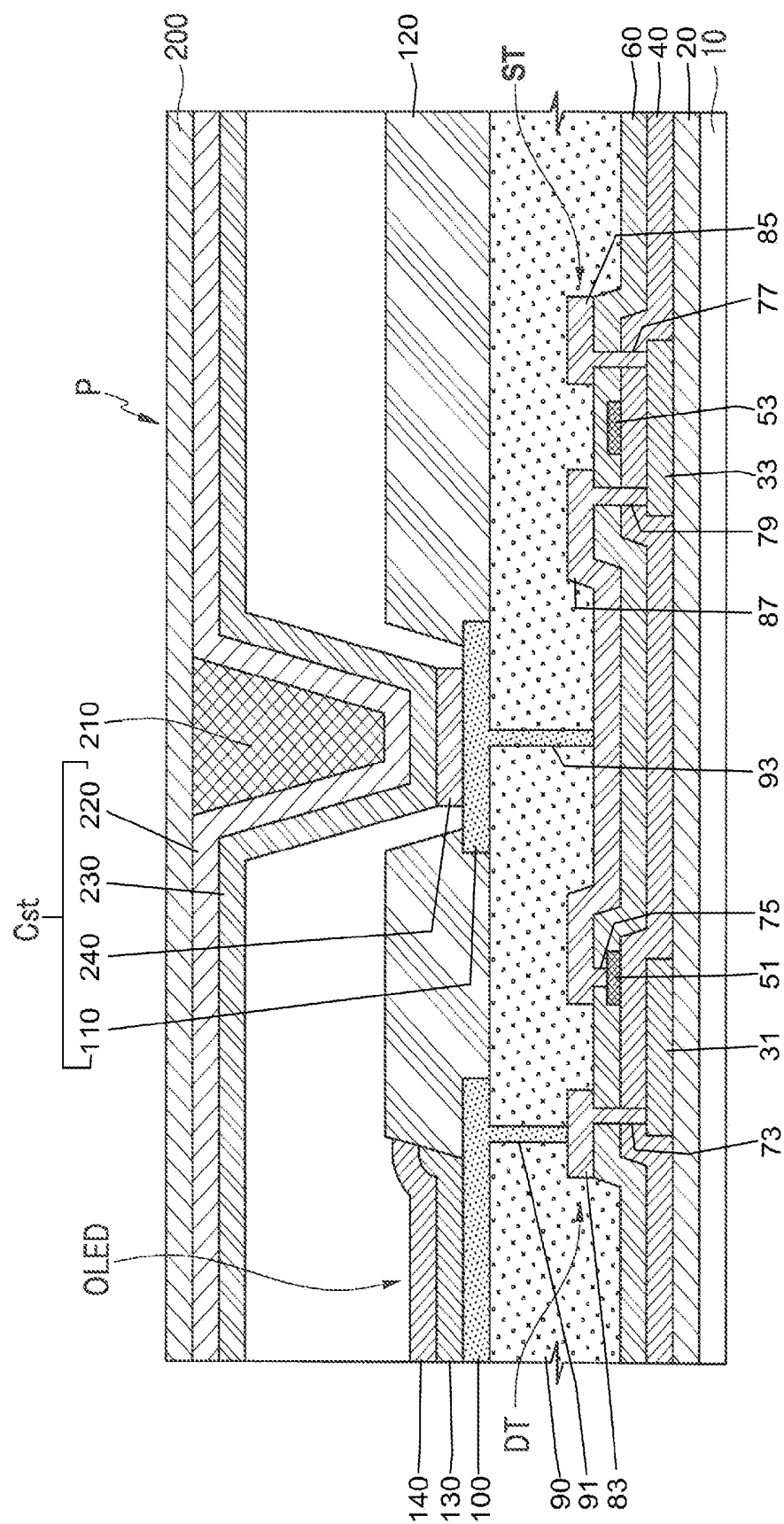
3
G
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FIG. 4A

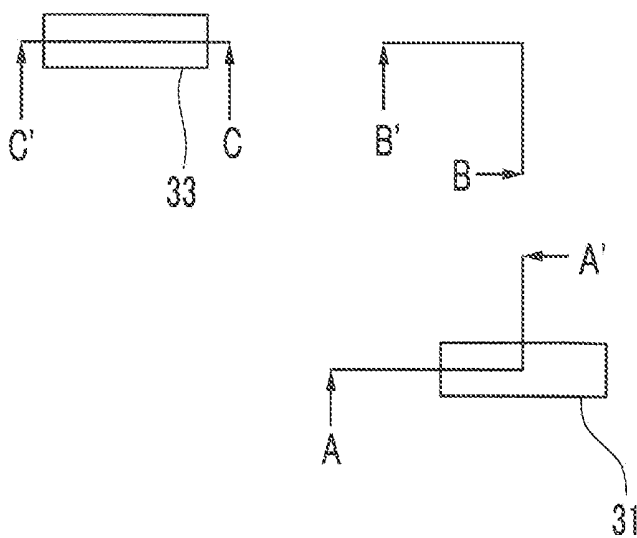


FIG. 4B

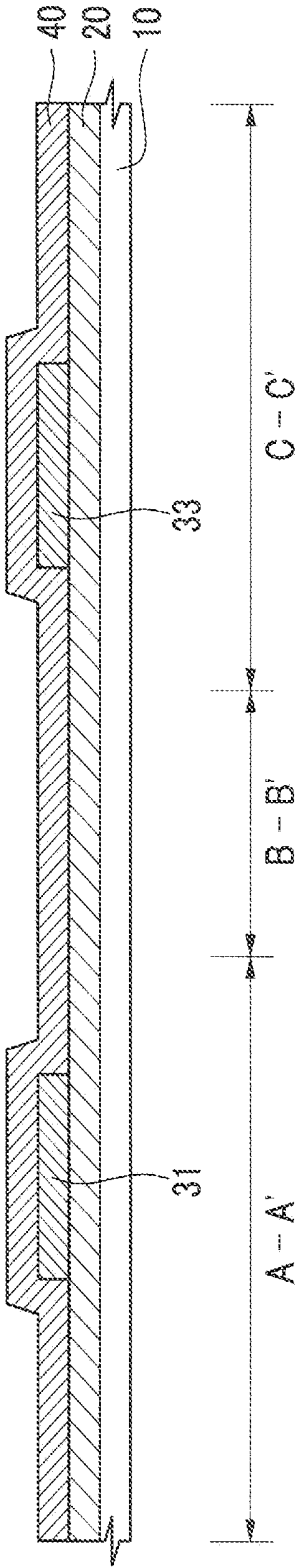


FIG.5A

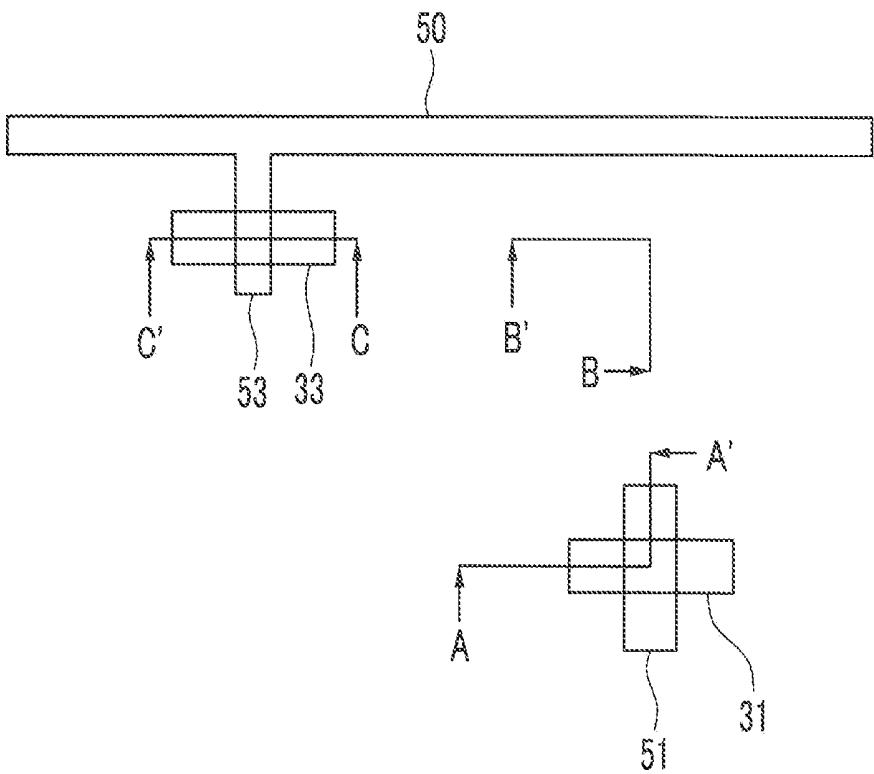


FIG. 5B

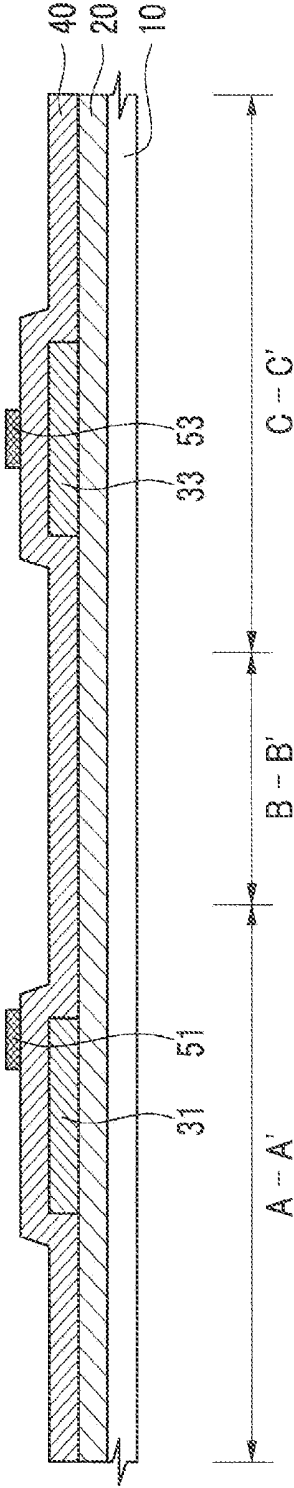


FIG. 6A

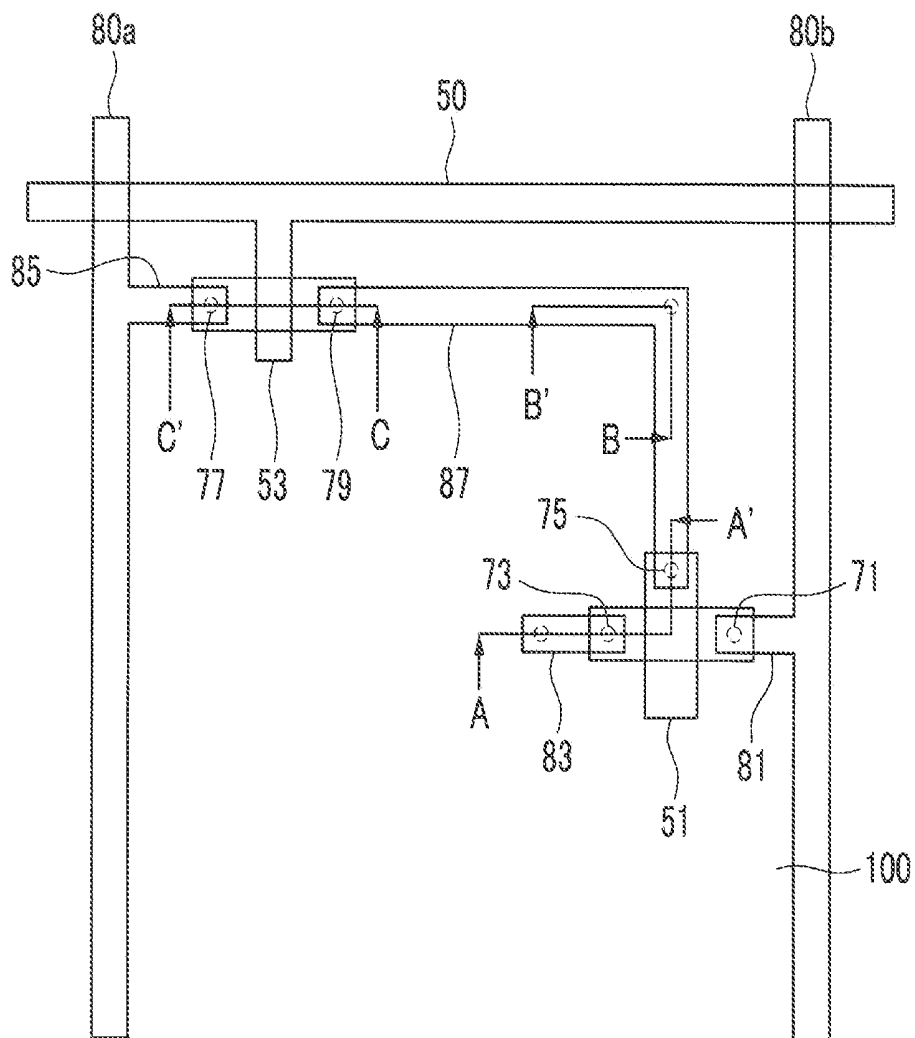


FIG. 6B

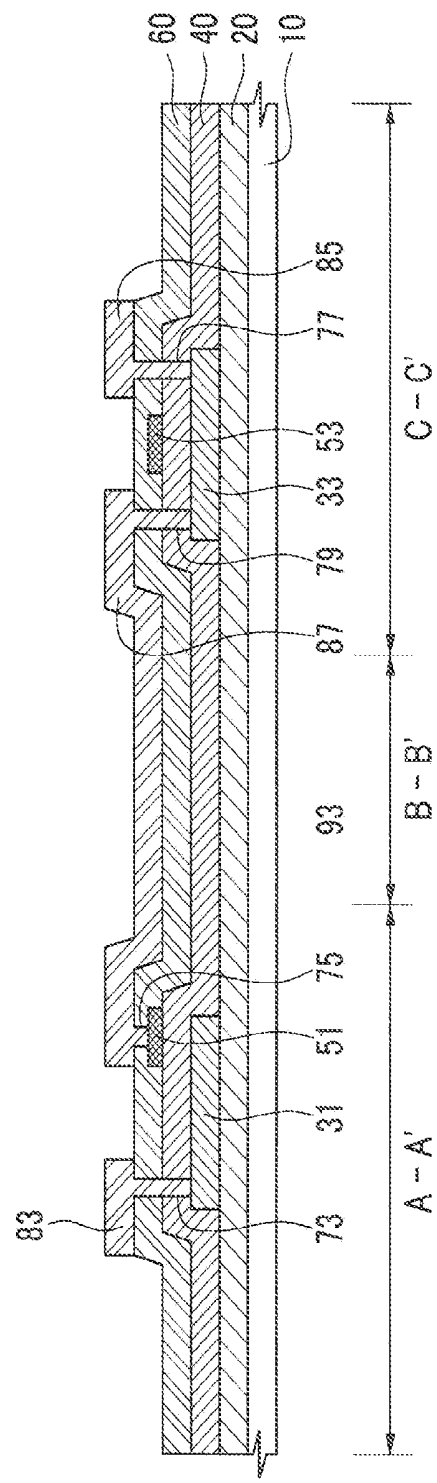


FIG. 7A

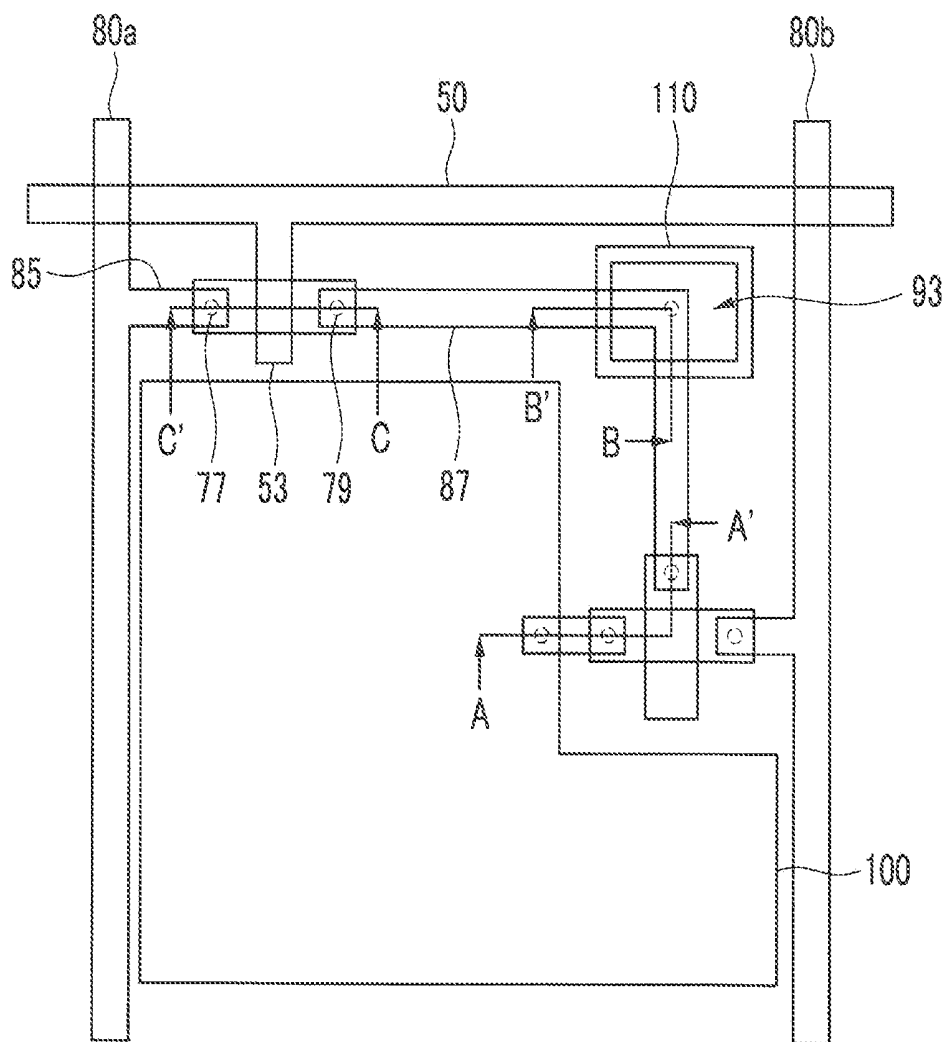


FIG. 7B

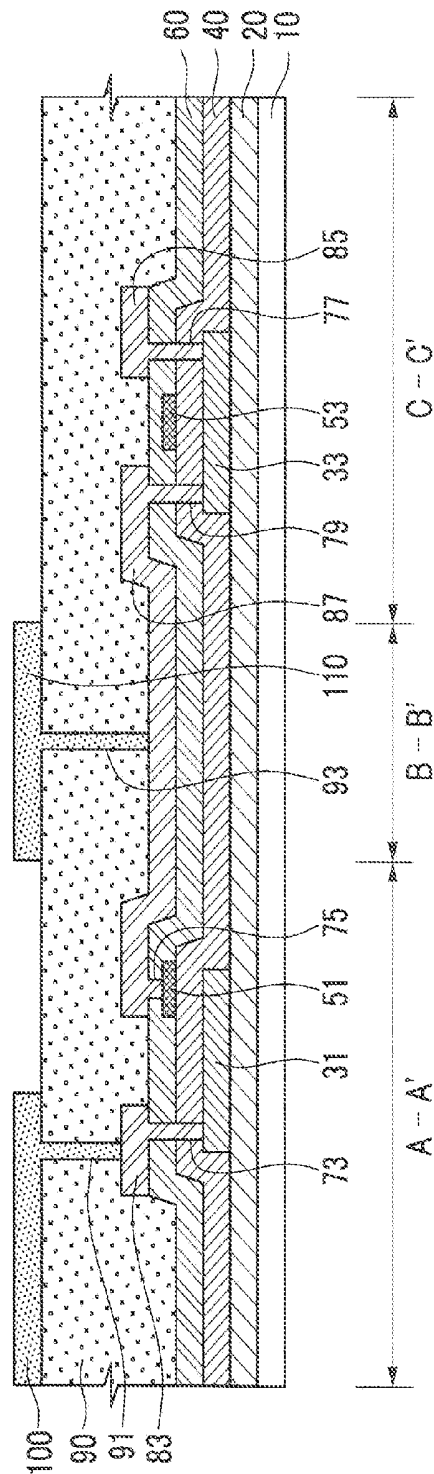


FIG. 8A

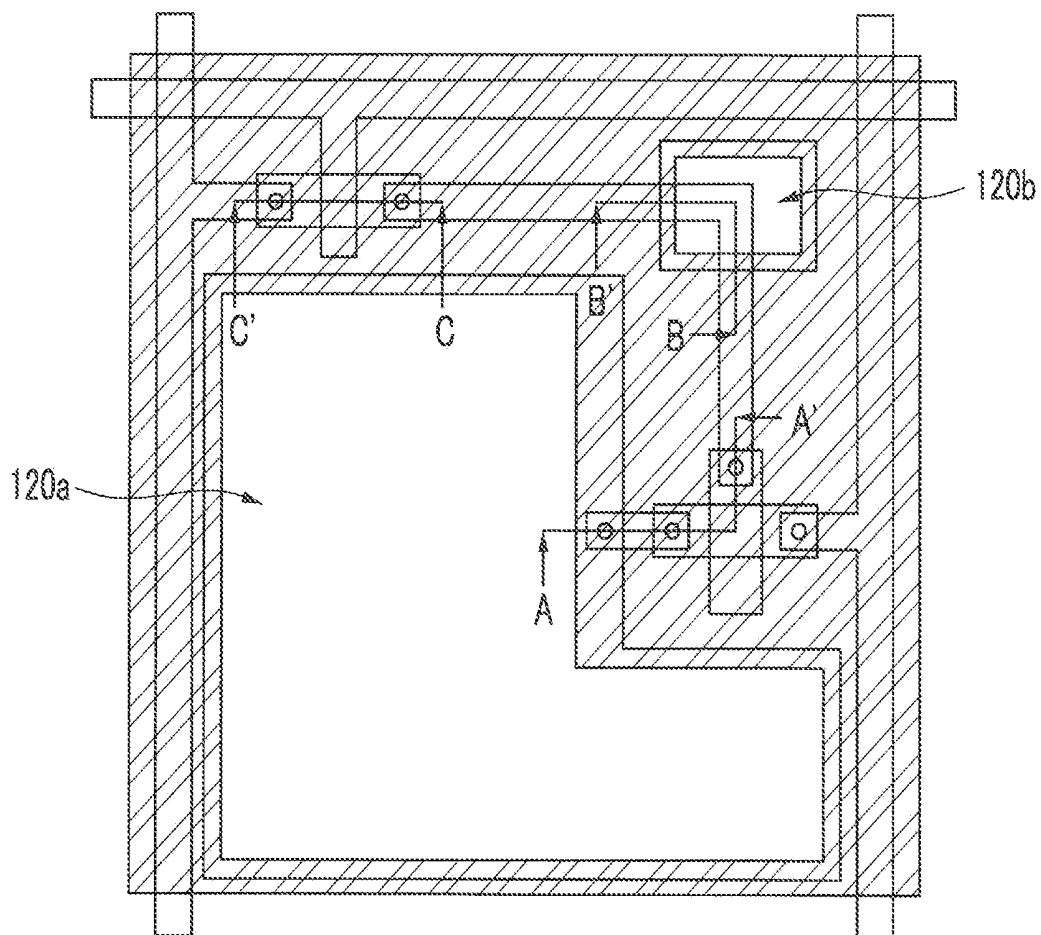


FIG. 8B

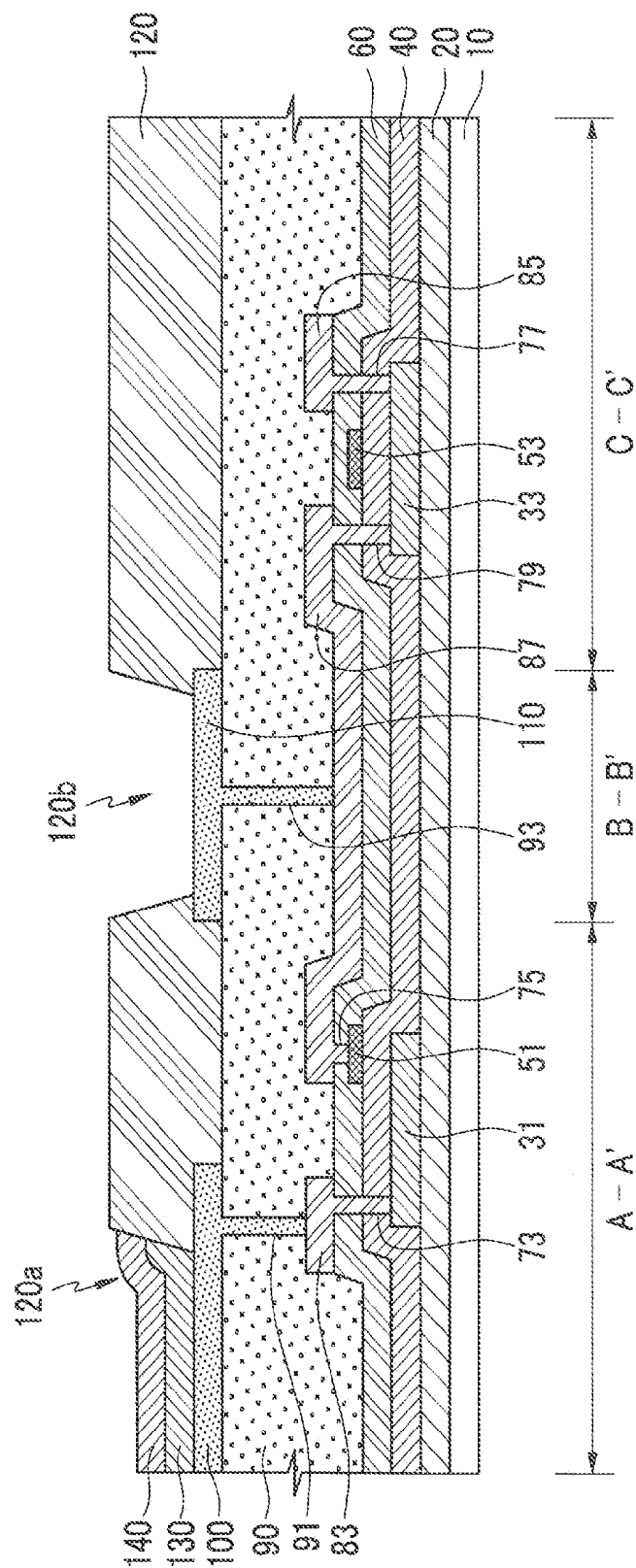


FIG. 9A

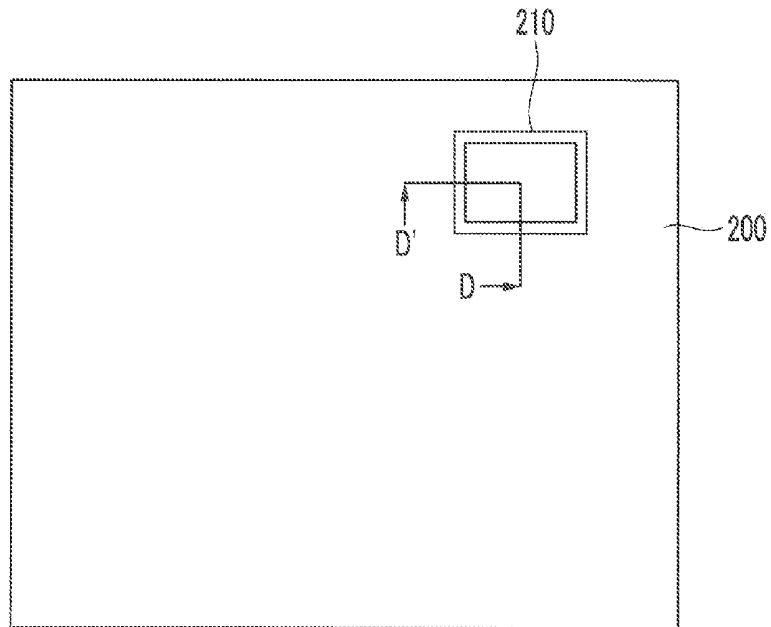


FIG. 9B

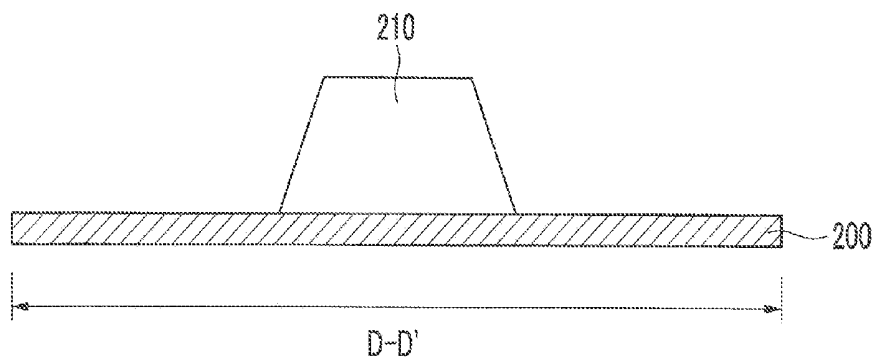


FIG. 10A

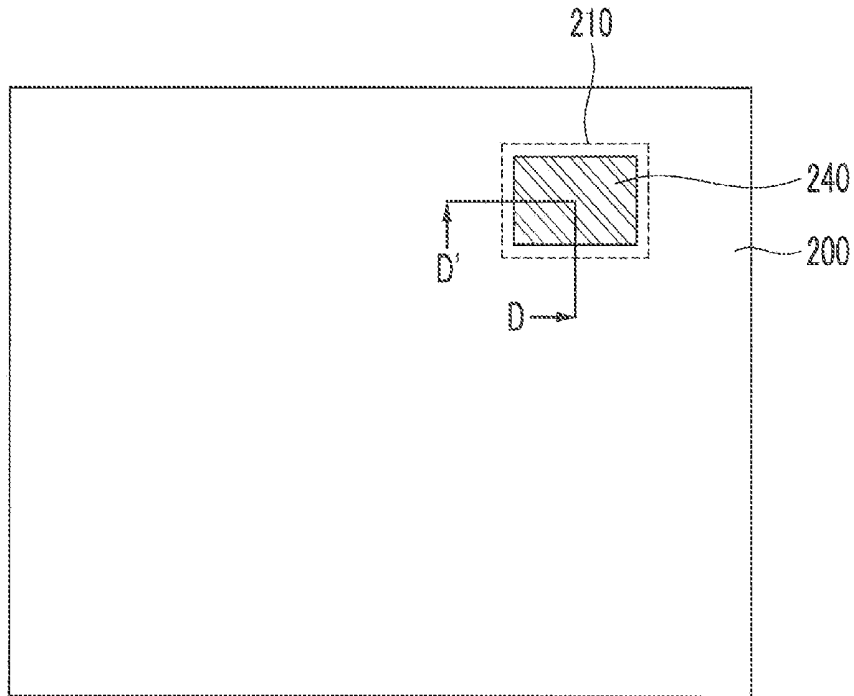


FIG. 10B

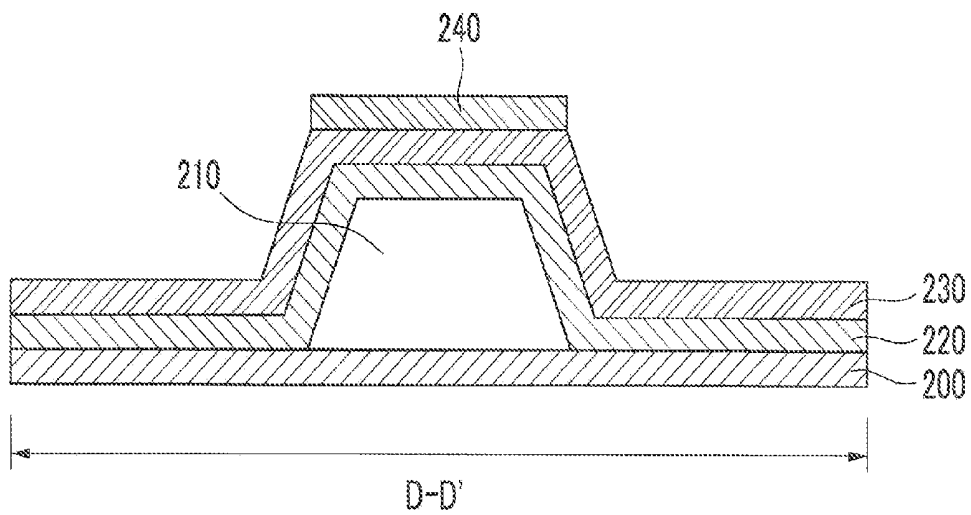
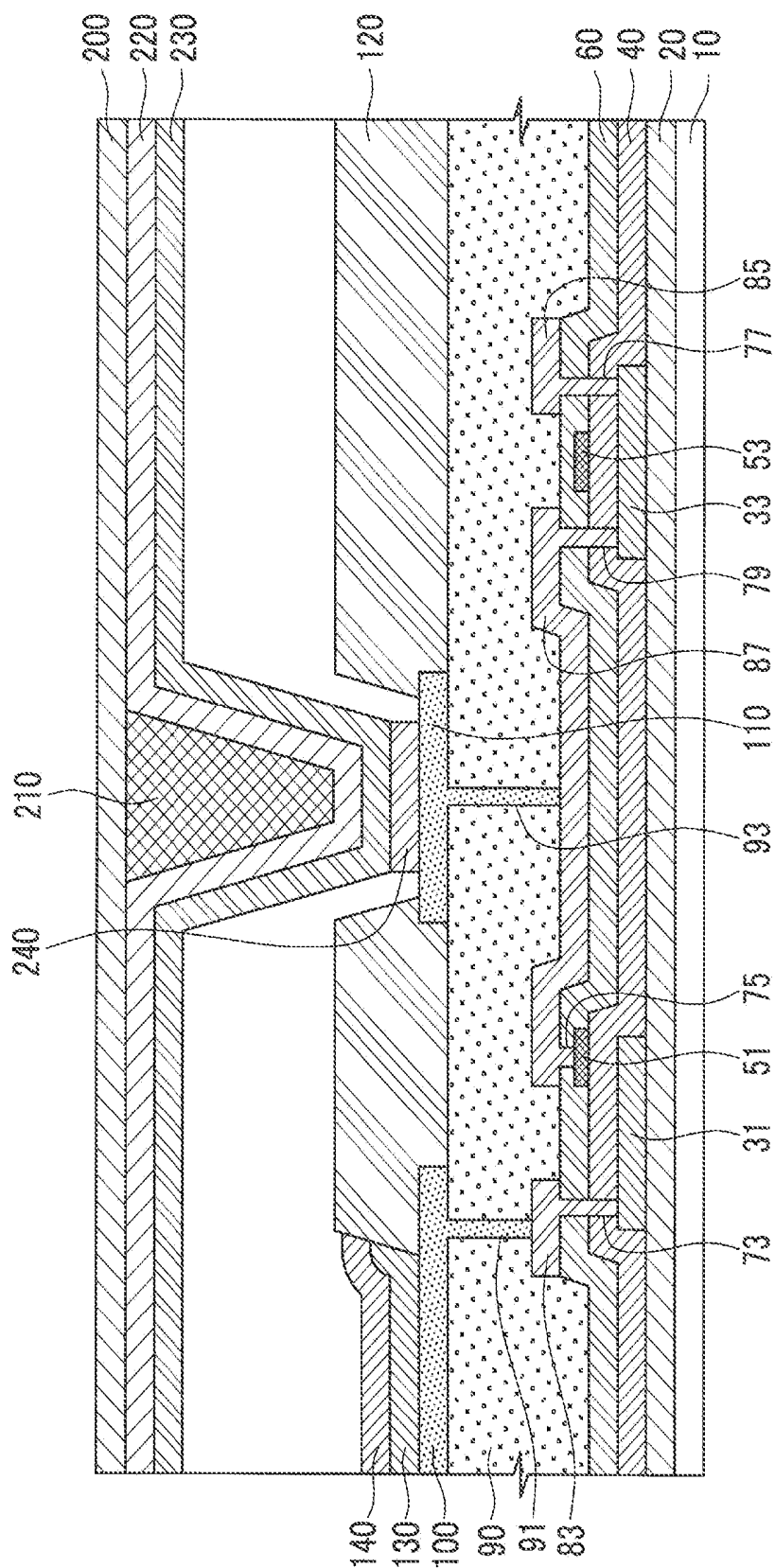


FIG. 11



METHOD OF MANUFACTURING AN ORGANIC LIGHT EMITTING DISPLAY

CLAIM OF PRIORITY

This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. § 119 from an application earlier filed in the Korean Intellectual Property Office on Feb. 8, 2010 and there duly assigned Serial No. 10-2010-0011511, and claims all benefits accruing under 35 U.S.C. § 120 from an application earlier filed in the U.S. Patent and Trademark Office on Nov. 12, 2010 and there duly assigned Ser. No. 12/945,373, now U.S. Pat. No. 8,441,181 issued on May 14, 2013.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The described technology relates generally to an organic light emitting display and a manufacturing method thereof capable of improving an aperture ratio.

2. Description of the Related Art

Among flat panel displays, an organic light emitting display is a self light emitting type of display that electrically excites an organic compound that emits light.

Since the organic light emitting display does not require a backlight as with a liquid crystal display, the organic light emitting display can become thin and light, and a manufacturing process of the organic light emitting display can be simplified. Further, the organic light emitting display can be fabricated at low temperature, have a high-speed response speed of 1 ms or less, and show characteristics such as low power consumption, wide viewing angle, and high contrast.

The organic light emitting display includes an organic emission layer between an anode and a cathode. Therefore, holes supplied from the anode and electrons supplied from the cathode are coupled to each other in the organic emission layer to form an exciton that is an electron-hole pair, causing the organic light emitting display to emit light by energy generated upon the exciton being restored to a ground state.

Generally, the organic light emitting display is manufactured by forming thin film transistors and an organic light emitting diode electrically connected with the thin film transistors on a substrate and thereafter, bonding the substrate to a sealing substrate.

The organic light emitting display manufactured as above operates as any one of a top emission type or a bottom emission type. The bottom emission type has a more stable diode than the top emission type, but has a lower aperture ratio than the top emission type.

The bottom emission type includes a light emitting area in addition to a transistor area, a capacitor area, and a wire area. Among them, only when the capacitor has a predetermined capacity or more, the capacitor may maintain signal data of one frame and may be compensated. However, it is difficult to decrease the size of the capacitor which occupies a large area.

Further, thinning the capacitor causes a short-circuit defect rate and a process distribution increase.

The above information disclosed in this Background section is only for enhancement of understanding of the background of the described technology, and therefore it may contain information that does not constitute prior art as per 35 U.S.C. § 102.

SUMMARY OF THE INVENTION

The described technology has been made in an effort to provide an organic light emitting display capable of improving an aperture ratio.

Further, the described technology has been made in an effort to provide a manufacturing method of an organic light emitting display capable of improving an aperture ratio.

An exemplary embodiment provides an organic light emitting display that includes a first substrate facing a second substrate and a plurality of pixels arranged between the first substrate and the second substrate, each of said pixels includes a plurality of thin film transistors, an organic light emitting diode, and a capacitor, wherein the plurality of thin film transistors and the organic light emitting diode are arranged on the first substrate and the capacitor is arranged on the second substrate, the plurality of thin film transistors and the capacitor being electrically connected to each other.

The capacitor of the display may include first lower electrode, also known as a first capacitor lower electrode, arranged on the first substrate and being electrically connected to the thin film transistors, the first capacitor lower electrode also being electrically connected to the capacitor.

The first capacitor lower electrode may be electrically connected to a gate electrode of one of the thin film transistors and a drain electrode of another of the thin film transistors. The capacitor may include a spacer arranged on the second substrate, a capacitor upper electrode arranged on the spacer and a dielectric layer arranged on the capacitor upper electrode.

The first capacitor lower electrode may contact the dielectric layer. The capacitor may also include second lower electrode, also known as a second capacitor lower electrode, arranged on the dielectric layer. The second capacitor lower electrode may contact the first capacitor lower electrode.

The display may also include first and second semiconductor layers each arranged on the first substrate, a gate insulating layer arranged on the first substrate that includes the first and second semiconductor layers, first and second gate electrodes arranged on the gate insulating layer and partially overlapping the first and second semiconductor layers, respectively, an interlayer insulating layer arranged on the first substrate that includes the first and second gate electrodes, the interlayer insulating layer being perforated by a contact hole to expose the first gate electrode, first source and drain electrodes and second source and drain electrodes arranged on the interlayer insulating layer, the second drain electrode being electrically connected to the exposed first gate electrode and a passivation layer arranged on the first substrate that includes the first source and drain electrodes and the second source and drain electrodes, the passivation layer may be perforated by first and second via holes exposing the first drain electrode and the second drain electrode respectively, the first capacitor lower electrode may be arranged on the passivation layer. The second drain electrode may extend to be electrically connected to the first gate electrode.

The display may also include a pixel electrode arranged on the passivation layer, a pixel defining layer arranged on the passivation layer and including first and second openings exposing the pixel electrode and the first capacitor lower electrode respectively, an organic layer arranged on the exposed pixel electrode and a counter electrode arranged on the organic layer. The first capacitor lower electrode may be electrically connected to the first gate electrode and the second drain electrode through the second via hole. The first capacitor lower electrode and the pixel electrode may be arranged on the same layer. The first capacitor lower electrode and the pixel electrode may be comprised of the same material.

According to another aspect of the present invention, there is provided a method of making an organic light emitting display, including forming a plurality of thin film transistors

and an organic light emitting diode on a first substrate, forming a capacitor on a second substrate and electrically connecting the plurality of thin film transistors and the capacitor to each other by bonding the first substrate to the second substrate. The forming of the organic light emitting diode on the substrate may include forming a first capacitor lower electrode on the first substrate that is electrically connected to the thin film transistors. The first capacitor lower electrode may be electrically connected to the capacitor. The forming of the capacitor on the second substrate may include forming a spacer on the second substrate, forming a capacitor upper electrode on the spacer and forming a dielectric layer on the capacitor upper electrode. The first capacitor lower electrode may contact the dielectric layer upon the bonding of the first substrate to the second substrate. The method may also include forming a second capacitor lower electrode on the dielectric layer. The first capacitor lower electrode may contact the second capacitor lower electrode upon the bonding of the first substrate to the second substrate.

Before the forming of the first capacitor lower electrode, the method may also include forming first and second semiconductor layers on the first substrate, forming a gate insulating layer on the first substrate that includes the first and second semiconductor layers, forming first and second gate electrodes on the gate insulating layer to partially overlap the first and second semiconductor layers, forming an interlayer insulating layer on the first substrate that includes the first and second gate electrodes, forming first to fifth contact holes by partially etching the gate insulating layer and the interlayer insulating layer, forming first source and drain electrodes and second source and drain electrodes on the interlayer insulating layer, the second drain electrode being electrically connected to the first gate electrode that is exposed by one of the contact holes, forming a passivation layer on the first substrate that includes the first source and drain electrodes and the second source and drain electrodes and etching the passivation layer to form first and second via holes, the first capacitor lower electrode being arranged on the passivation layer. The second drain electrode may extend to be electrically connected to the first gate electrode. The method may also include forming a pixel electrode on the passivation layer, forming a pixel defining layer on the passivation layer, the pixel defining layer being perforated by first and second openings that expose the pixel electrode and the first capacitor lower electrode respectively, forming an organic layer on the exposed pixel electrode and forming a counter electrode on the organic layer. The pixel electrode and the first capacitor lower electrode may be produced in the same process.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

FIG. 1 is a perspective view schematically illustrating one example of an organic light emitting display according to an exemplary embodiment;

FIG. 2 is a circuit diagram illustrating an enlarged unit pixel area of FIG. 1;

FIG. 3 is a cross-sectional view illustrating a lamination structure of the unit pixel area of FIG. 1;

FIGS. 4A to 8B are plan views and cross-sectional views for describing a method for forming thin film transistors and an organic light emitting diode on a first substrate;

FIGS. 9A to 10B are plan views and cross-sectional views for describing a method for forming a capacitor on a second substrate; and

FIG. 11 is a cross-sectional view for describing the connection relationship between thin film transistors and a capacitor.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, an organic light emitting display and a manufacturing method thereof according to exemplary embodiments will be described with reference to the accompanying drawings. The structure of the organic light emitting display described below is just an exemplary embodiment for describing the present invention and the present invention is in no way limited to the exemplary embodiment. In addition, the structure of the organic light emitting display may be variously modified and still be within the scope of the present invention.

FIG. 1 is a perspective view schematically illustrating one example of an organic light emitting display according to an exemplary embodiment, FIG. 2 is a circuit diagram illustrating an enlarged unit pixel area P of FIG. 1, and FIG. 3 is a cross-sectional view illustrating a lamination structure of the unit pixel area P of FIG. 1.

Referring to FIGS. 1 to 3, the organic light emitting display according to the exemplary embodiment includes a plurality of signal lines D1 to Dm, S1 to Sn, ELVDD, and ELVSS arranged in a matrix and pixels P11 to Pnm formed at intersection areas where data lines D1 to Dm, S1 to Sn, ELVDD, and ELVSS intersect each other and between first and second substrates 10 and 200 that face each other.

The signal lines are constituted by data lines D1 to Dm to which data signals are applied, power supply lines ELVDD and ELVSS to which power is always applied while the organic light emitting display is being driven, and gate lines S1 to Sn to which scan signals for selecting the pixels P11 to Pnm are applied.

A unit pixel P includes two thin film transistors TFTs, a capacitor Cst, and an organic light emitting diode OLED. One of the two thin film transistors is a switching TFT (ST) and the other one is defined as a driving TFT (DT) due to their roles.

The switching TFT (ST) is turned on or turned off in response to a scan signal from the gate line Sn. When the switching TFT (ST) is turned on, the switching TFT (ST) transfers a data signal from the data line Dm. The capacitor Cst includes an upper electrode connected to the first power supply line ELVDD and a lower electrode connected with a drain electrode of the switching TFT (ST) and a gate electrode of the driving TFT. The capacitor Cst stores a data signal received through the switching TFT (ST) and serves to sustain a gate-source voltage Vgs of the driving TFT (DT) for a predetermined time.

The drain electrode of the switching TFT (ST) is connected to the gate electrode of the driving TFT (DT), the first power supply line ELVDD is connected to a source electrode of the driving TFT (DT) and an anode electrode of the organic light emitting diode OLED is connected to a drain electrode of the driving TFT (DT).

Therefore, the driving TFT (DT) generates driving current corresponding to the data signal transferred through the switching TFT (ST), and outputs the driving current to the organic light emitting diode OLED.

The organic light emitting diode OLED includes an anode, a cathode, and a light emitting layer positioned between the anode and the cathode. The anode is connected to the drain electrode of the driving TFT (DT) and the cathode is con-

nected to a second power supply line ELVSS to perform a light emitting operation depending upon the driving current.

In this case, the thin film transistors DT and ST and the organic light emitting diode OLED are formed on the first substrate **10**, and the capacitor Cst is formed on the second substrate **200**.

According to the exemplary embodiment, a method of manufacturing an organic light emitting display includes a diode substrate forming step of forming first and second thin film transistors and an organic light emitting diode on a first substrate **10**, a capacitor substrate forming step of forming a capacitor on a second substrate **200**, and a bonding step of bonding the second substrate **200** to the first substrate **10** to electrically connect the capacitor to the first and second thin film transistors.

First, referring to FIGS. **4A** to **8B**, a method of forming the first and second thin film transistors and the organic light emitting diode on the first substrate will be described. In this case, figures with a suffix of 'A' (e.g., FIG. **4A**, FIG. **5A** etc.) are plan views after each process is performed, and figures with a suffix of 'B' (e.g., FIGS. **4B**, **5B**, . . .) are cross-sectional views taken along lines A-A', B-B', and C-C' of the corresponding figure having the 'A' suffix. However, in a figure having an 'A' suffix, a film formed on the overall surface of the first substrate and a film patterned after the film is formed may not be shown for convenience, but said missing film may be visible in the corresponding figures having the 'B' suffix. Further, a 'transistor area', a 'capacitor area', and a 'light emitting area' used in the following description do not have determined positions and define predetermined positions where the transistor, the capacitor, and the organic light emitting diode are formed.

Referring to FIGS. **4A** and **4B**, a buffer layer **20** is formed on the overall surface of the first substrate **10**, and an amorphous silicon layer (not shown) is formed on the buffer layer **20**. In this case, the first substrate **10** may be a transparent insulating substrate made of glass, quartz, sapphire, and the like and the buffer layer **20** may be formed by depositing silicon oxide or silicon nitride via a PECVD technique.

The buffer layer **20** prevents the amorphous silicon layer (not shown) from being contaminated by impurities diffused from the first substrate **10** upon crystallization of the amorphous silicon layer (not shown) which is a post process.

Thereafter, the amorphous silicon layer (not shown) is crystallized by using a technique such as excimer laser annealing (ELA), sequential lateral solidification (SLS), metal induced crystallization (MIC), or metal induced lateral crystallization (MILC), which is a general crystallization technique. The crystallized silicon layer is then patterned by using an etching process to produce each of first and second semiconductor layers **31** and **33** within the transistor area of the unit pixel. In some cases, the crystallization process can be omitted, such that the first and the second semiconductor layers **31** and **33** may be made out of amorphous silicon. Alternatively, one semiconductor layer may be crystallized and the other semiconductor layer may not be crystallized.

After formation of first and second semiconductor layers **31** and **33**, a gate insulating layer **40** is formed on the overall surface of the first substrate **10** that includes the first and the second semiconductor layers **31** and **33**. The gate insulating layer **40** may be made out of silicon oxide, silicon nitride, or a laminated structure thereof.

Next, referring to FIGS. **5A** and **5B**, a gate electrode material (not shown) is applied onto the gate insulating layer **40**, and thereafter, the gate electrode material is patterned by an etching process to form first and second gate electrodes **51** and **53** in the transistor area. In addition, a scan line **50** into

which a scan signal is input, is also formed upon the formation of the first and second gate electrodes **51** and **53**, the second gate electrode **53** being connected to the scan line **50**.

The first and second gate electrodes **51** and **53** partially overlapped the first and second semiconductor layers **31** and **33**. Portions of the first and second semiconductor layers **31** and **33** that are overlapped by the first and second gate electrodes **51** and **53** represent the channel region of the first and second semiconductor layers.

The first and second gate electrodes **51** and **53** may be a single layer of aluminum (Al), an aluminum alloy such as aluminum-neodymium (Al—Nd) or a plurality of layers in which an aluminum alloy layer is laminated on a chrome (Cr) or molybdenum (Mo) alloy layer.

Next, referring to FIGS. **6A** and **6B**, an interlayer insulating layer **60** is formed at the upper part of the first substrate **10** that includes the first and second gate electrodes **51** and **53**. The interlayer insulating layer **60** may be a silicon nitride layer or a silicon oxide layer.

Thereafter, the gate insulating layer **40** and the interlayer insulating layer **60** are partially etched to form first to fifth contact holes **71**, **73**, **75**, **77**, and **79**.

A first source area and a first drain area of the first semiconductor layer **31** are exposed by the first and second contact holes **71** and **73**, the first gate electrode **51** is exposed by the third contact hole **75** and a second source area and a second drain area of the second semiconductor layer **33** are exposed by the fourth and fifth contact holes **77** and **79**.

Thereafter, after a metallic film (not shown) is formed on the interlayer insulating layer **60**. The metallic film is patterned through an etching process to form first source and drain electrodes **81** and **83** and second source and drain electrodes **85** and **87**.

The first source and drain electrodes **81** and **83** are connected to the source and drain areas respectively of the first semiconductor layer **31** through the first and second contact holes **71** and **73**. The second source and drain electrodes **85** and **87** are connected to the source and drain areas respectively of the second semiconductor layer **33** through the fourth and fifth contact holes **77** and **79**. In this case, the second drain electrode **87** extends so that it is electrically connected to the first gate electrode **51** via the third contact hole **75**.

A data line **80a** to which a data signal is applied, and a power supply voltage line **80b** to which power supply voltage is applied, are produced from the same metal film used to produce the first and second source and drain electrodes **81**, **83**, **85** and **87**. The second source electrode **85** is formed by extending the data line **80a**, and the first source electrode **81** is formed by extending the power supply voltage line **80b**. Therefore, the power supply voltage is applied to the first source electrode **81** and the data signal is applied to the second source electrode **85**.

The metallic film (not shown) may form a single layer that includes a material selected from Mo, W, MoW, AlNd, Ti, Cu, a Cu alloy, Ag, and an Ag alloy. The metallic film may also be a lamination structure selected from a group formed in a dual-layer structure including a layer of one of Mo, Cu, Al, or Ag which are low-resistance materials or a multi-layer structure of two layers or more in order to reduce wiring resistance.

Next, referring to FIGS. **7A** and **7B**, a passivation layer **90** having a predetermined thickness is formed on the overall surface of the first substrate **10**. The passivation layer **90** may be a single layer such as an organic layer, an inorganic layer or a lamination structure of an inorganic layer and an organic layer.

Thereafter, the passivation layer **90** is partially etched through an etching process to form first and second via holes **91** and **93**. Upon said etching, the first drain electrode **83** is partially exposed by the first via hole **91** and the second drain electrode **87** is partially exposed by the second via hole **93**.

Thereafter, a metallic film (not shown) is formed on the passivation layer **90** that includes the plurality of via holes **91** and **93**, and the metallic film is patterned through an etching process to produce a pixel electrode **100** in the light emitting area and a first capacitor lower electrode (i.e. first lower electrode of the capacitor) **110** in the capacitor area.

The pixel electrode **100** is connected to the first drain electrode **83** through the first via hole **91**, and the first lower electrode **110** of the capacitor is electrically connected to the second drain electrode **87** and the first gate electrode **51** through the second via hole **93**.

In this case, in the case of the bottom emission type, the pixel electrode **100** may be a transparent electrode made out of a material selected from a group consisting of indium tin oxide (ITO), indium zinc oxide (IZO), tin oxide (TO), and zinc oxide (ZnO).

Meanwhile, in the case of the top emission type, the pixel electrode **100** may be a reflective electrode that includes a reflective layer made out of a material selected from a group consisting of Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, and alloys thereof, and a transparent layer made out of a material selected from a group consisting of indium tin oxide (ITO), indium zinc oxide (IZO), tin oxide (TO), and zinc oxide (ZnO) laminated thereon. In addition, the transparent layer may instead be formed on the bottom of the reflective layer. However, in the present invention, the configuration of the pixel electrode is not limited.

The first lower electrode **110** of the capacitor is connected to a capacitor formed on the second substrate **200** to be described below, and is also electrically connected to the first and second thin film transistors. The first lower electrode **110** of the capacitor is not limited to a particular location, but is preferably positioned at a location that does not reduce the range (i.e., size) of the light emitting area.

Meanwhile, it is advantageous that the first lower electrode **110** of the capacitor be produced in the same process and include the same material as that of the pixel electrode **100**, but in the present invention, the material and process of the first lower electrode of the capacitor is in no way so limited.

Next, referring to FIGS. **8A** and **8B**, a pixel defining layer **120**, including first and second openings **120a** and **120b**, is formed on the passivation layer **90** to partially expose the pixel electrode **100** and the first lower electrode **110** of the capacitor, respectively.

The pixel defining layer **120** may be made out of a material selected from a group consisting of polyimide, benzocyclobutene series resin, spin on glass (SOG), and acrylate.

Thereafter, an organic layer **130** is formed in the first opening **120a**, and a counter electrode **140** is formed on the organic layer **130**.

The organic layer **130** may be produced by using a low molecule deposition technique or a thermal transferring technique, and may include at least one layer selected from an organic emission layer, an electron injection layer, an electron transport layer, a hole injection layer, a hole transport layer and a hole suppress layer.

In the case of the bottom emission type, the counter electrode **140** is reflective and may be made out of a material selected from a group consisting of Li, Ca, LiF/Ca, LiF/Al, Al, Mg, and alloys thereof.

Meanwhile, in the case of the top emission type, the counter electrode **140** may be configured to include a material

having a small work function, such as a material selected from a group consisting of Li, Ca, LiF/Ca, LiF/Al, Al, Mg, and a Mg alloy, and may have a small thickness in the range of 5 to 30 nm. The counter electrode **140** may additionally include a transparent layer of indium tin oxide (ITO), indium zinc oxide (IZO), and the like having a low-resistance characteristic laminated onto the thin, small work function layer.

In the above description, the method of forming the thin film transistors and the organic light emitting diode on the first substrate **10** has been described. Hereinafter, a method of forming the capacitor on the second substrate **200** will now be described.

First, referring to FIGS. **9A** and **9B**, a spacer **210** is formed in a capacitor area of the second substrate **200** at a location that corresponds to the capacitor area B-B' of the first substrate **10** in which the first capacitor lower electrode **110** of the capacitor is arranged. In this case, when the spacer **210** is too high, the space between the first substrate **10** and the second substrate **200** becomes larger, such that the entire thickness of the organic light emitting display is increased. Therefore, the height of the spacer **210** is properly selected within a process range. However, the position of the capacitor area D-D' on the second substrate **200** is not limited, and the capacitor area represents a predetermined area where the capacitor is formed.

Meanwhile, the upper end of the spacer **210** may be flattened such that it becomes easier to form the capacitor in a subsequent process. The spacer **210** merely serves to facilitate electrical connection between the capacitor and the thin film transistors. When the spacer **210** is not required, the spacer **210** may not be formed.

Next, referring now to FIGS. **10A** and **10B**, an upper electrode of the capacitor **220** is formed on the second substrate **200** where the spacer **210** is arranged, and a power supply voltage is applied to the upper electrode **220** of the capacitor. In this case, the upper electrode **220** of the capacitor may be produced by forming a metallic layer on the overall surface of the second substrate **200**, or by patterning a part of the metallic layer formed on the overall surface. In the case of the bottom emission type, the upper electrode **220** of the capacitor may be formed on the overall surface of the second substrate **200** or may be patterned, but in the case of the top emission type, the upper electrode **220** of the capacitor is preferably patterned in order not to reduce the range of the light emitting area.

Thereafter, a dielectric layer **230** of the capacitor is formed on the capacitor upper electrode **220**. The dielectric layer **230** may be an insulating layer such as a silicon oxide layer, a silicon nitride layer or a high-dielectric inorganic insulating layer. The dielectric layer **230** may be formed on the overall surface of the upper electrode **220** of the capacitor, or may be formed only within the capacitor area D-D' on the upper electrode **220** of the capacitor.

Thereafter, a capacitor lower electrode **240** of the capacitor is formed in the capacitor area D-D' and on the dielectric layer **230**. The second lower electrode **240** of the capacitor may be produced by depositing a metallic layer on the overall surface of the second substrate **200** where the dielectric layer **230** is formed, and patterning the deposited metallic layer. FIGS. **9A** to **10B** illustrate one method of forming the capacitor on the second substrate **200**, but the present invention is in no way so limited.

Turning now to FIG. **11**, FIG. **11** is a cross-sectional view of a pixel for describing the connection relationship between the thin film transistors and the capacitor. Referring to FIG. **11**, when the organic light emitting display is completed by bonding the first substrate **10** to the second substrate **200**, so

that the first lower electrode **110** of the capacitor on the first substrate **10** contacts the capacitor formed on the second substrate **200** to electrically connect the thin film transistors to the capacitor. Upon the first substrate **10** being bonded to the second substrate **200**, the first lower electrode **110** of the capacitor of the first substrate **10** contacts the second lower electrode **240** of the capacitor of the second substrate **200**.

However, in the exemplary embodiment, it has been described as an example that the first lower electrode **110** of the capacitor of the first substrate **10** and the second lower electrode **240** of the capacitor of the second substrate **200** form the lower electrode of the capacitor. In a variation, the lower electrode of the capacitor may include only the first lower electrode **110** of the capacitor without the second lower electrode **240** of the capacitor. In this variation, the first lower electrode **110** of the capacitor directly contacts the dielectric layer **230**.

According to the exemplary embodiments, the capacitor is not formed on the substrate that the thin film transistors and the organic light emitting diode are formed. As a result, even the area where the capacitor is formed may be formed as part of the light emitting area, thereby improving an aperture ratio.

While this disclosure has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood to those skilled in the art that the invention is not limited to the disclosed embodiments. Therefore, the invention is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims

What is claimed is:

1. A method of manufacturing an organic light emitting display, comprising:

forming a plurality of thin film transistors and an organic light emitting diode on a first substrate;
forming a capacitor on a second substrate; and
electrically connecting the plurality of thin film transistors and the capacitor to each other by bonding the first substrate to the second substrate.

2. The method of claim **1**, wherein the forming of the organic light emitting diode on the first substrate includes forming a first lower electrode of the capacitor on the first substrate that is electrically connected to the thin film transistors.

3. The method of claim **2**, wherein the first lower electrode of the capacitor is electrically connected to the capacitor.

4. The method of claim **1**, wherein the forming of the capacitor on the second substrate includes:

forming a spacer on the second substrate;
forming upper electrode of the capacitor on the spacer; and
forming a dielectric layer on the upper electrode of the capacitor.

5. The method of claim **4**, wherein the first lower electrode of the capacitor contacts the dielectric layer upon the bonding of the first substrate to the second substrate.

6. The method of claim **4**, further comprising forming a second lower electrode of the capacitor on the dielectric layer.

7. The method of claim **6**, wherein the first lower electrode of the capacitor contacts the second lower electrode of the capacitor upon the bonding of the first substrate to the second substrate.

8. The method of claim **2**, before the forming of the first lower electrode of the capacitor, the method further comprises:

forming first and second semiconductor layers on the first substrate;
forming a gate insulating layer on the first substrate that includes the first and second semiconductor layers;

forming first and second gate electrodes on the gate insulating layer to partially overlap the first and second semiconductor layers;

forming an interlayer insulating layer on the first substrate that includes the first and second gate electrodes;

forming first to fifth contact holes by partially etching the gate insulating layer and the interlayer insulating layer;

forming first source and drain electrodes and second source and drain electrodes on the interlayer insulating layer, the second drain electrode being electrically connected to the first gate electrode that is exposed by one of the contact holes;

forming a passivation layer on the first substrate that includes the first source and drain electrodes and the second source and drain electrodes; and

etching the passivation layer to form first and second via holes, the first lower electrode of the capacitor being arranged on the passivation layer.

9. The method of claim **8**, wherein the second drain electrode extends to be electrically connected to the first gate electrode.

10. The method of claim **8**, further comprising:

forming a pixel electrode on the passivation layer;
forming a pixel defining layer on the passivation layer, the pixel defining layer being perforated by first and second openings that expose the pixel electrode and the first lower electrode of the capacitor respectively;

forming an organic layer on the exposed pixel electrode; and

forming a counter electrode on the organic layer.

11. The method of claim **10**, wherein the pixel electrode and the first lower electrode of the capacitor are produced in the same process.

12. The method of claim **10**, wherein the pixel electrode and the first lower electrode of the capacitor are comprised of the same material.

13. The method of claim **1**, the display being a front emission display where an image is viewed from a side corresponding to the second substrate and not from a side corresponding to the first substrate.

14. The method of claim **2**, wherein the first lower electrode of the capacitor is formed at a same time and of a same material as that of a pixel electrode of the organic light emitting diode.

15. The method of claim **1**, wherein the capacitor is arranged at a location corresponding to the thin film transistors and not the organic light emitting diode.

16. The method of claim **1**, wherein the bonding occurs after the forming of the thin film transistors and the organic light emitting diode on the first substrate, and after the forming of the capacitor on the second substrate.

17. The method of claim **2**, further comprising:

forming a passivation layer on the thin film transistors on the first substrate;

forming a pixel electrode of the diode and a first lower electrode of the capacitor on the passivation layer, the pixel electrode and the first lower electrode being formed simultaneously and being comprised of a same material; and

forming a pixel defining layer on the passivation layer, the pixel defining layer being perforated by first and second openings that expose the pixel electrode and the first lower electrode of the capacitor respectively.

18. A method of manufacturing an organic light emitting display, comprising:

forming a plurality of thin film transistors and an organic light emitting diode on a first substrate;

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forming portions of a capacitor on a second and different substrate; and then

electrically connecting the plurality of thin film transistors to the portions of the capacitor by bonding the second substrate to the first substrate.

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19. The method of claim **18**, wherein the method further includes forming a first layer of lower electrode of the capacitor on the first substrate, wherein the forming of the portions of the capacitor on the second and different substrate comprises:

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forming an upper electrode of the capacitor on the second substrate;

forming a dielectric layer of the capacitor on the upper electrode; and

forming a second layer of the lower electrode of the capacitor on the dielectric layer, wherein the second layer of the lower electrode of the capacitor is directly bonded to the first layer of the lower electrode of the capacitor upon the bonding together of the first and second substrates.

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20. The method of claim **18**, wherein the forming of the organic light emitting diode on the first substrate comprises: depositing a passivation layer on the thin film transistors formed on the first substrate; and

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forming simultaneously a pixel electrode of the organic light emitting diode and a first lower electrode of the capacitor on the passivation layer on the first substrate.

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专利名称(译)	制造有机发光显示器的方法		
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[标]申请(专利权)人(译)	三星显示有限公司		
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摘要(译)

一种导致改善的孔径比的有机发光显示器及其制造方法。有机发光显示器包括布置在第一和第二基板之间的多个像素，每个所述像素包括多个薄膜晶体管，有机发光二极管和电容器。薄膜晶体管和有机发光二极管形成在第一基板上，电容器形成在第二基板上，并且薄膜晶体管和电容器在第一基板接合到第二基板时彼此电连接。

